# EN0-001 Q&As

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**QUESTION 1**

Which THREE of the following items should be preserved by software when entering dormant mode? (Choose three)

A. Current Program Status Register (CPSR)

B. Contents of the Level 2 data cache

C. The Floating Point Status and Control Register (FPSCR)

D. All User mode general-purpose registers

E. The CP15 Multiprocessor Affinity Register

F. Contents of the Level 1 data cache

Correct Answer: ACD

**QUESTION 2**

According to the AAPCS, how many bytes are used to store a C variable of type \\'int\\' in memory?

A. 1 byte

B. 2 bytes

C. 4 bytes

D. 8 bytes

Correct Answer: C

**QUESTION 3**

Which of the following is an advantage of the single-step debug technique?

A. It allows a complete trace of real-time program execution to be captured

B. It reduces the number of pins required to connect the debugger to the processor

C. It allows examination of the system state before and after execution of a statement

D. It requires only one change to the program source code

Correct Answer: C

**QUESTION 4**

A re-entrant interrupt handler would typically be used to:

A. Allow an external interrupt to interrupt an SVC handler

B. Reduce response time for higher priority interrupts

C. Allow an interrupt handler to be relocated in memory

D. Avoid the need for an interrupt handler to use a stack.

Correct Answer: B

**QUESTION 5**

According to the AAPCS, which of the following statements is TRUE with regard to preservation of register values by a function?

A. A function must preserve R0-R3 and R12

B. A function must preserve R4-R11 andR13

C. No registers may be corrupted by any function

D. All registers may be corrupted by any function

Correct Answer: B

**QUESTION 6**

The following ARM instruction can be used to return from an exception:

movs pc, lr

Apart from the program counter, which register is updated by this instruction?

A. Ir

B. r0

C. CPSR

D. SCTLR

Correct Answer: C

**QUESTION 7**

Consider the following instruction sequence: STR r0, [r2] ; instruction A DSB ADD r0, r1, r2 ; instruction B LDR r3, [r4] ; instruction C

SUB r5, r6, #3 ; instruction D

At what point will execution pause until the STR access is complete?

A. After instruction A and before the DSB

B. After the DSB and before instruction B

C. After instruction B and before instruction C

D. After instruction C and before instruction D

Correct Answer: B

**QUESTION 8**

How many ARM core registers and PSRs (Program Status Registers) are available to the programmer in User mode on a Cortex-A9?

A. 16

B. 17

C. 18

D. 32

Correct Answer: B

**QUESTION 9**

When using an Operating System, which instruction is used by user code to request a service from the kernel?

A. BLX

B. RFEFD

C. SRSFD

D. SVC

Correct Answer: D

**QUESTION 10**

In an experiment, the time taken for an application to complete a given task is measured using a stopwatch. Which THREE of the following make up the total time? (Choose three)

A. The time spent waiting for I/O operations

B. The time taken to download the program via the debugger

C. The time taken for memory accesses

D. The time taken for the CPU to execute instructions

E. The time taken to compile the source code

F. The time taken to perform instruction tracing

Correct Answer: ACD

**QUESTION 11**

What type of instruction is used for cache maintenance operations?

A. Dedicated ARM instructions

B. Dedicated Thumb instructions

C. CP14 instructions

D. CP15 instructions

Correct Answer: D

**QUESTION 12**

What is the maximum value of the immediate field in an ARM SVC instruction?

A. 0x0

B. 0xF

C. 0xFF

D. 0xFFFFFF

Correct Answer: D

**QUESTION 13**

Which of the following register values would cause an unaligned access when the instruction LDRH r0, [r1] is executed?

A. R0=0x100, R1 =0x1000

B. R0=0x100, R1=0x1002

C. R0=0x101, R1=0x1002

D. R0=0x101. R1=0x1003

Correct Answer: D

**QUESTION 14**

In a Cortex-A9 MPCore cluster with four processors, which of the processors can be interrupted by a software-generated interrupt?

A. Any processor in the cluster

B. Only the processor raising the software-generated interrupt

C. Only processors outside the cluster

D. Any processor except the one raising the software-generated interrupt

Correct Answer: A

**QUESTION 15**

The Memory Protection Unit (MPU) of Cortex-R4 performs which of the following tasks?

A. Translates virtual addresses to physical addresses

B. Generates parity information to detect soft errors in memory

C. Performs access permission checks

D. Permits the system to be divided into secure and normal worlds, through the use of ARM\\'s TrustZone technology

Correct Answer: C