# EN0-001 Q&As

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**QUESTION 1**

What are the values of the NZCV bits in the CPSR after executing the following instructions?

LDR R0, = 0xFFFFFFFF

ADDS R0, R0, #1

A. 0101

B. 0110

C. 1001

D. 1010

Correct Answer: B

**QUESTION 2**

Which one of these statements is TRUE about code running on final hardware without a debugger attached?

A. It must start executing from RAM

B. RAM must be initialized before reset

C. Exception handlers must execute from ROM or flash memory

D. It must not execute semihosting SVC or BKPT instructions

Correct Answer: D

**QUESTION 3**

Which of the following sequences of stages comprise the ARM7TDMI three-stage pipeline?

A. Fetch, Decode, Execute

B. Decode, Fetch, Execute

C. Execute, Fetch, Decode

D. Fetch, Execute, Execute

Correct Answer: A

**QUESTION 4**

If the performance of an application remains unchanged when the core clock speed of a Cortex-A9 processor is

reduced, what can you deduce about the system?

A. The Clocks Per Instruction (CPI) of the processor has increased

B. The processor is NOT the limiting factor on performance

C. Instruction cache utilization has improved

D. The core has stopped carrying out speculative data memory accesses

Correct Answer: B

**QUESTION 5**

When an ARMv7-A MPCore system is in SMP mode, which of the following TWO operations can the processor handle automatically? (Choose two)

A. Coherency management between all L1 data caches

B. Broadcast of some inner-shared cache and TLB maintenance operations

C. Broadcast of some outer-shared cache and TLB maintenance operations

D. Coherency management between all L1 instruction caches

E. Coherency management between all external caches

Correct Answer: AB