EN0-001 Q&As

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QUESTION 1

A re-entrant interrupt handler would typically be used to:

A. Allow an external interrupt to interrupt an SVC handler

B. Reduce response time for higher priority interrupts

C. Allow an interrupt handler to be relocated in memory

D. Avoid the need for an interrupt handler to use a stack.

Correct Answer: B

QUESTION 2

An advantage of removable flash memory over built-in flash memory is that:

A. Storage can be easily replaced, for example to increase capacity.

B. It is quicker to access, providing far greater bandwidth for read operations.

C. It has a longer life, indicated by being rated for a higher number of write cycles.

D. It takes up less physical space in a device, and does not require any space on the printed circuit board.

Correct Answer: A

QUESTION 3

Which one of these statements is TRUE about code running on final hardware without a debugger attached?

A. FIQ exceptions must not be taken

B. The instruction cache must be enabled

C. Global variables must be initialized to zero

D. The Reset Vector must reside in non-volatile memory

Correct Answer: D

QUESTION 4

In a hardware system that runs software providing secure systems, which of the following describes the behavior of external memory and peripherals?

A. They are not accessible when the processor is in Non-secure state

B. They cannot know whether the processor is performing a Secure or Non-secure access

C. They can use the Secure or Non-secure status of the access to decide what response to give

D. They are required to give an ERROR response when Secure code accesses Non-secure locations in memory

Correct Answer: C

QUESTION 5

A message passing system between two CPUs is implemented using data stored in a shared area of

memory. To pass a message, the first CPU executes the instructions:

```
    STR r3, [r1]  ;// set new message at address pointed to by r1
A
    STR r0, [r2]  ;// send flag to indicate message is ready to read
B
```

The second CPU receives the message using the instructions:

```
loop
    LDR r12, [r2] ;// load the message available flag
C
    CMP r12, #1   ;// test the flag
    BNE loop      ;// if the flag is clear, loop.
D
    LDR r3, [r1]  ;// load the new message
```

On both CPUs, r1 = 0x5000 and r2 = 0x6000. At which of the points A, B, C and D must Data Memory Barrier (DMB) instructions be placed in order to ensure messages are passed reliably and efficiently?

A. A only

B. C only

C. B and C

D. A and D

Correct Answer: D