



# EN0-001<sup>Q&As</sup>

ARM Accredited engineer

## Pass ARM EN0-001 Exam with 100% Guarantee

Free Download Real Questions & Answers **PDF** and **VCE** file from:

<https://www.pass4itsure.com/en0-001.html>

100% Passing Guarantee  
100% Money Back Assurance

Following Questions and Answers are all new published by ARM  
Official Exam Center

- ⚙️ **Instant Download** After Purchase
- ⚙️ **100% Money Back** Guarantee
- ⚙️ **365 Days** Free Update
- ⚙️ **800,000+** Satisfied Customers





### QUESTION 1

Under which of the following circumstances would a DSB instruction be used?

- A. In a multi-threaded system, when two threads need to be synchronized at a particular point
- B. When accessing a peripheral, it is necessary to halt until the memory access is complete
- C. When it is necessary to temporarily disable interrupts while carrying out a particular memory access
- D. In a multiprocessor system, when it is necessary to halt one of the cores while the other completes a critical task

Correct Answer: B

---

### QUESTION 2

In which of the following scenarios would cache maintenance operations be necessary in an ARMv7 system?

- A. Before executing code that uses the NEON instruction set
- B. Before handling an interrupt request raised by an external device
- C. Before checking the status of a semaphore
- D. Before reading cacheable memory that has been written to by an external bus master

Correct Answer: D

---

### QUESTION 3

In a Cortex-A9 MPCore cluster with four processors, which of the processors can be interrupted by a software-generated interrupt?

- A. Any processor in the cluster
- B. Only the processor raising the software-generated interrupt
- C. Only processors outside the cluster
- D. Any processor except the one raising the software-generated interrupt

Correct Answer: A

---

### QUESTION 4

When using the default ARM tool-chain libraries for bare-metal applications. I/O functionality is rerouted and handled by a connected debugger. This is often referred to as semihosting. Which one of the following explanations BEST describes how this feature can be implemented by a debugger?



- A. The library directly sends I/O requests to the debugger using the JTAG connection
- B. While the target is running, the debugger processes I/O requests from a shared queue in memory
- C. The I/O library calls rely on an Ethernet connection to redirect the requests to the debugger
- D. The I/O library calls generate an exception that is trapped and handled by the debugger

Correct Answer: D

---

#### QUESTION 5

In a Cortex-A processor, assume an initial value of R1 = 0x80004000.

If the following instruction causes a data abort, what value will R1 contain on entry to the abort handler?

LDR R0, [R1, #8]!

- A. 0x80003FF8
- B. 0x80004000
- C. 0x80004008
- D. R1 contents are unpredictable

Correct Answer: B

[EN0-001 Practice Test](#)

[EN0-001 Study Guide](#)

[EN0-001 Exam Questions](#)